Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A latch circuit for synchronizing a pulse signal for latching image data with a clock signal, comprising:

a first input comprising the pulse signal;

a second input comprising the clock signal; and

an output comprising the pulse signal in synchronization with the clock signal, wherein the clock signal has an amplitude smaller than an amplitude of the pulse signal outputted from the latch circuit.

B1 cont

Claim 2 (original): A latch circuit as claimed in claim 1, further comprising a first circuit having a voltage holding function and a second circuit having a level shifting function, the first and second circuits being constructed so as to own some common elements.

Claim 3 (original): A latch circuit as claimed in claim 2, wherein the latch circuit is supplied with a power potential, and an element for controlling the voltage holding function or the level shifting function of the input signal is provided between the power potential and the second circuit.

Claims 4-17 (canceled)

Claim 18 (currently amended): A shift register circuit having a plurality of latch circuits for transmitting a pulse signal for latching image data in synchronization with a clock signal, each of the latch circuits comprising:

a clock signal input control section for executing control to input and stop the supplied clock signal, wherein the clock signal has an amplitude smaller than an amplitude of the pulse signal; and

an output comprising the pulse signal in synchronization with the clock signal.

Claim 19 (original): A shift register circuit as claimed in claim 18, wherein the clock signal inputted to the latch circuits is only either one of a clock signal of a specified cycle and an antiphase signal of the clock signal.

Claim 20 (original): A shift register circuit as claimed in claim 18, wherein an output signal of each of the latch circuits is inputted to the latch circuit of the succeeding stage via a first transfer gate and inputted to the latch circuit of the preceding stage via a second transfer gate, and a scanning direction is controlled by selectively making conductive the first or second transfer gate by means of an external signal.

B1 Cont

Claim 21 (original): A shift register circuit as claimed in claim 18, wherein an output signal of each of the latch circuits is inputted to the latch circuit of the succeeding stage via a buffer circuit.

Claims 22-36 (canceled)

Claim 37 (previously presented): A CMOS logical circuit which performs a logical operation based on a plurality of input signals, the CMOS logical circuit comprising:

a first input signal having a first amplitude; and

a second input signal having a second amplitude;

wherein the amplitude of at least one of the input signals is smaller than a drive voltage of the CMOS logical circuit.

Claim 38 (original): A logical circuit as claimed in claim 37 comprising two electric current paths each of which has a circuit consisting of at least one n-type transistor and a circuit consisting of at least one p-type transistor, wherein

as concerns the circuit having one of the n-type transistor and the p-type transistor,

the one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit outputting a logical operation result similar to that of the logical circuit, and

the other electric current path is provided with a circuit having the same construction as that of a circuit having a p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit, and

as concerns the circuit having the transistor of the other channel type,

a gate electrode of the transistor provided on the one electric current path and that of the transistor provided on the other electric current path are connected to drain electrodes of the counterparts.

B1 cont

Claim 39 (original): A logical circuit as claimed in claim 37 comprising two electric current paths each of which has a circuit consisting of at least one n-type transistor and a circuit consisting of at least one p-type transistor, wherein

as concerns the circuit having one of the n-type transistor and the p-type transistor,

the one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit outputting a logical operation result similar to that of the logical circuit, and

the other electric current path is provided with a circuit having the same construction as that of a circuit having a p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit, and

as concerns the circuit having the transistor of the other channel type,

each of the two electric current paths is provided with a transistor to which at least one of the input signals is inputted to a gate electrode and a transistor at a power source side of each thereof such that a gate electrode of the transistor provided on the one electric current path is connected to an output portion of the other electric current path, and a gate electrode of the

transistor provided on the other electric current path is connected to an output portion of the one electric current path.

Claim 40 (original): A logical circuit as claimed in claim 37 comprising two electric current paths each of which has a circuit consisting of at least one n-type transistor and a circuit consisting of at least one p-type transistor, wherein

as concerns the circuit having one of the n-type transistor and the p-type transistor of the logical circuit,

the one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit outputting a logical operation result similar to that of the logical circuit, and

B1 cont

the other electric current path is provided with a circuit having the same construction as that of a circuit having a p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit, and

as concerns the circuit having the transistor of the other channel type,

the one electric current path is provided with the circuit having the same construction as that of the circuit having the p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit,

the other electric current path is provided with the circuit having the same construction as that of the circuit having the n-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit,

each of the two electric current paths is provided with a transistor at a power source side thereof such that a gate electrode of the transistor provided on the one electric current path is connected to an output portion of the other electric current path, and a gate electrode of the transistor provided on the other electric current path is connected to an output portion of the one electric current path.

Claim 41 (original): A logical circuit as claimed in claim 39, wherein in the n-type circuit or the p-type circuit, a signal having a smaller amplitude than a plurality of the signals is inputted to

one transistor positioned farther from the output portion than the other transistor that is connected in series with the one transistor.

Claim 42 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to drain electrodes of the counterparts and connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a drain electrode connected to a source electrode of the third transistor, and a source electrode connected to a second supply potential;

B1 cont

a fifth transistor having a gate electrode connected to a third input terminal, a drain electrode connected to the first output terminal, and a source electrode connected to the second supply potential; and

a sixth transistor having a gate electrode connected to a fourth input terminal, a drain electrode connected to the first output terminal, and a source electrode connected to the second supply potential;

wherein

signals to be inputted to the first and third input terminals are inverse to each other in phase, and signals to be inputted to the second and fourth input terminals are inverse to each other in phase, and

the first and second transistors are of a channel type different from that of the other transistors.

Claim 43 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to drain electrodes of the counterparts and connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a drain electrode connected to a source electrode of the third transistor, and a source electrode connected to a second supply potential;

a fifth transistor having a gate electrode connected to a third input terminal, a drain electrode connected to the second output terminal, and a source electrode connected to the second supply potential;

a sixth transistor having a gate electrode connected to a fourth input terminal and a source electrode connected to the second supply potential;

a seventh transistor having a gate electrode connected to a fifth input terminal and a source electrode connected to the second supply potential; and

B1 cont

an eighth transistor having a gate electrode connected to a sixth input terminal, a drain electrode connected to the first output terminal, and a source electrode connected to the drain electrode of the sixth transistor and that of the seventh transistor,

wherein

signals to be inputted to the first and fourth input terminals are inverse to each other in phase, signals to be inputted to the second and fifth input terminals are inverse to each other in phase, and signals to be inputted to the third and sixth input terminals are inverse to each other in phase, and

the first and second transistors are of a channel type different from that of the other transistors.

Claim 44 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to drain electrodes of the counterparts and connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a drain electrode connected to a source electrode of the third transistor, and a source electrode connected to a second supply potential;

a fifth transistor having a gate electrode connected to a third input terminal, a drain electrode connected to the second output terminal, and a source electrode connected to the second supply potential; and

a sixth transistor having a gate electrode connected to a fourth input terminal and a drain electrode connected to the first output terminal;

a seventh transistor having a gate electrode connected to a fifth input terminal and a drain electrode connected to the first output terminal; and

an eighth transistor having a gate electrode connected to a sixth input terminal, a drain electrode connected to a source electrode of the sixth transistor and that of the seventh transistor, and a source electrode connected to the second supply potential,

B1 cont

wherein

signals to be inputted to the first and fifth input terminals are inverse to each other in phase, signals to be inputted to the second and fourth input terminals are inverse to each other in phase, and signals to be inputted to the third and sixth input terminals are inverse to each other in phase, and

the first and second transistors are of a channel type different from that of the other transistors.

Claim 45 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal, a source electrode connected to a drain electrode of the first transistor, and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to the drain electrode of a second transistor, and a drain electrode connected to the first output terminal;

a fifth transistor having a gate electrode connected to a third input terminal and a drain electrode connected to the second output terminal;

a sixth transistor having a gate electrode connected to the first input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the fifth transistor;

a seventh transistor having a gate electrode connected to a fourth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal; and

B1 cont

an eighth transistor having a gate electrode connected to the second input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal,

wherein

signals to be inputted to the first and second input terminals are inverse to each other in phase, signals to be inputted to the third and fourth input terminals are inverse to each other in phase, and

the first through fourth transistors are of a channel type different from that of the other transistors.

Claim 46 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal, a source electrode connected to a drain electrode of the first transistor, and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to the drain electrode of a first transistor, and a drain electrode connected to the second output terminal;

a fifth transistor having a gate electrode connected to a third input terminal, and a source electrode connected to a drain electrode of the second transistor;

a sixth transistor having a gate electrode connected to a fourth input terminal, a source electrode connected to a drain electrode of the fifth transistor, and a drain electrode connected to the first output terminal;

a seventh transistor having a gate electrode connected to a fifth input terminal and a drain electrode connected to the second output terminal;

an eighth transistor having a gate electrode connected to the second input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the seventh transistor,

B1 cont

a ninth transistor having a gate electrode connected to a sixth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal, and

a 10th transistor having a gate electrode connected to the fourth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal,

wherein

signals to be inputted to the first and third input terminals are inverse to each other in phase, and signals to be inputted to the second and fourth input terminals are inverse to each other in phase, and

the first through sixth transistors are of a channel type different from that of the other transistors.

Claim 47 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal, a source electrode connected to a drain electrode of the first transistor, and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to a drain electrode of the second transistor, and a drain electrode connected to the first output terminal;

a fifth transistor having a gate electrode connected to a third input terminal, and a drain electrode connected to the second output terminal;

a sixth transistor having a gate electrode connected to the first input terminal, a source electrode connected to a second supply potential, and a drain electrode connected to a source electrode of the fifth transistor;

a seventh transistor having a gate electrode connected to a fourth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the second output terminal;

B1 cont

an eighth transistor having a gate electrode connected to a fifth input terminal, and a drain electrode connected to the first output terminal,

a ninth transistor having a gate electrode connected to the second input terminal, and a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the eighth transistor, and

a 10th transistor having a gate electrode connected to a sixth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the eighth transistor,

wherein

signals to be inputted to the first and second input terminals are inverse to each other in phase, signals to be inputted to the third and sixth input terminals are inverse to each other in phase, and signals to be inputted to the fourth and fifth input terminals are inverse to each other in phase, and

the first through fourth transistors are of a channel type different from that of the other transistors.

Claim 48 (original): A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a source electrode connected to a drain electrode of the first transistor;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to a drain electrode of the third transistor, and a drain electrode connected to the second output terminal;

a fifth transistor having a gate electrode connected to a third input terminal, a source electrode connected to a drain electrode of the third transistor, and a drain electrode connected to the second output terminal;

a sixth transistor having a gate electrode connected to a fourth input terminal, a source electrode connected to a drain electrode of the second transistor, and a drain electrode connected to the first output terminal;

B1 cont

a seventh transistor having a gate electrode connected to a fifth input terminal and a source electrode connected to the drain electrode of the second transistor;

an eighth transistor having a gate electrode connected to a sixth input terminal, a source electrode connected to a drain electrode of the seventh transistor, and a drain electrode connected to the first output terminal;

a ninth transistor having a gate electrode connected to a seventh input terminal and a drain electrode connected to the second output terminal;

a 10th transistor having a gate electrode connected to an eighth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the ninth transistor,

an 11th transistor having a gate electrode connected to a ninth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the second output terminal,

a 12th transistor having a gate electrode connected to a 10th input terminal and a drain electrode connected to the first output terminal;

a 13th transistor having a gate electrode connected to an 11th input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the 12th transistor, and

a 14th transistor having a gate electrode connected to a 12th input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the source electrode of the 12th transistor,

wherein

signals to be inputted to the first and fourth input terminals are inverse to each other in phase, signals to be inputted to the second and sixth input terminals are inverse to each other in phase, and signals to be inputted to the third and fifth input terminals are inverse to each other in phase, and

the first through eighth transistors are of a channel type different from that of the other transistors.

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Claim 49 (original): A logical circuit as claimed in claim 37, wherein at least one of the input signals is inputted through a transfer transistor for controlling an input of the signals.

Claim 50 (original): A logical circuit as claimed in claim 49, wherein a malfunction prevention transistor is connectedly provided between a specified supply potential and a gate electrode of a transistor to which a signal controlled by the transfer transistor is inputted, and

the gate electrode of the malfunction prevention transistor is connected to a supply potential different from the special supply potential.

Claim 51 (original): A logical circuit as claimed in claim 49, wherein a malfunction prevention transistor is connectedly provided between a specified supply potential and a gate electrode of a transistor to which a signal controlled by a transfer transistor is inputted, and

a signal having a phase inverse to that of a signal to be inputted to the transfer transistor is inputted to a gate electrode of the malfunction prevention transistor.

Claim 52 (original): A logical circuit as claimed in claim 49, wherein any one of the input signals is inputted to a gate electrode of a transfer transistor.

Claim 53 (original): An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the data signal line drive circuit and/or the scanning signal line drive circuit has the logical circuit as claimed in claim 37.

Claims 54-57 (canceled)

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Claim 58 (original): An image display device as claimed in claim 53, wherein the data signal line drive circuit and/or the scanning signal line drive circuit is formed on a substrate identical to that of the pixels.

Claim 59 (original): An image display device as claimed in claim 58, wherein an active element that constitutes at least one of the signal line drive circuits and the pixels is a polysilicon thin-film transistor.

Claim 60 (original): An image display device as claimed in claim 59, wherein the active element is formed through a process at a temperature of not higher than 600°C.

Claim 61 (previously presented): An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the data signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

Claim 62 (previously presented): An image display device as claimed in claim 61, wherein in the logical circuit constituting the data signal line drive circuit and the scanning signal line drive circuit, an output signal of the shift register circuit is inputted to a gate electrode of the transfer transistor.

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Claim 63 (previously presented): An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

Claim 64 (previously presented): An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as at least one part of a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and one of a plurality of control signals inputted from outside as input signals and

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outputting signals simultaneously to a plurality of shift register circuits having a different combination.